Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2023/24)
Machine Structures 2 course
Kara Abdelaziz professor

Problem set 0 solution
(introductory concepts)

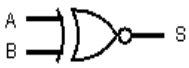
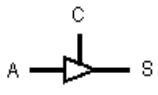
Exercise 01 :

1) The definition of logic gates.

A: Logic gates are physical (real), elementary (indivisible) electronic components used in digital electronics. They are assembled in composition to form logic circuits (combinational circuits and sequential circuits). Each logic gate electrically performs a basic boolean operation (and, or, not...etc). Generally a logic gate has 2 (or more) inputs and a single output. In digital electronics often the logic value 0 is represented by 0 volts and the logic value 1 is represented by 5 volts.

2) The table of logic gates :

Gate	Symbol	Truth table	Description
AND		A B S 0 0 0 0 1 0 1 0 0 1 1 1	It is the **and** logic : S = A·B
OR		A B S 0 0 0 0 1 1 1 0 1 1 1 1	It is the **or** logic : S = A+B
NOT		A S 0 1 1 0	It is the **not** logic : S = $\overline{A}$

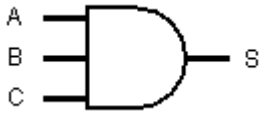
<table>
<tr>
<td>NAND</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>B</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td>
<td>It is the not-and logic : S = $\overline{A \cdot B}$</td>
</tr>
<tr>
<td>NOR</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>B</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td>
<td>It is the not-or logic : S = $\overline{A+B}$</td>
</tr>
<tr>
<td>XOR</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>B</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td>
<td>It is the exclusive-or logic : S = A⊕B</td>
</tr>
<tr>
<td>XNOR</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>B</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
<td>It is the not-exclusive-or logic :
S = $\overline{A \oplus B}$ = A⊗B</td>
</tr>
<tr>
<td>buffer</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>S</th></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>
</td>
<td>It is the buffer, a gate that doesn't do any logical operation, it is used to reduce the speed of the signal in some situations :
S = A</td>
</tr>
<tr>
<td>tristate buffer</td>
<td> 
</td>
<td>
<table>
<tr><th>A</th><th>C</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>Z</td></tr>
<tr><td>1</td><td>0</td><td>Z</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
<td>It is the tristate buffer, used to produce the Z logic signal :
$\begin{cases} if\,(C=0) \Rightarrow S=Z \\ if\,(C=1) \Rightarrow S=A \end{cases}$</td>
</tr>
</table>

(A,B are inputs. S is the output. C for the command)

Remarks :

1. Buffers are mainly used as regulators during the timing study of a digital circuit, timing study is not covered by this course.
2. The tristate buffer and the Z signal will be explained later in the next problem set.

3) The AND3 gate is an AND gate with 3 inputs.

<table>
<tr><th>Gate</th><th>Symbol</th><th>Truth table</th></tr>
<tr><td>AND3</td><td> 
</td><td>
<table>
<tr><th>A</th><th>B</th><th>C</th><th>S</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
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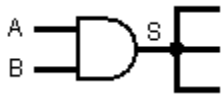
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

As noted before, the number 3 in the name AND3 is the number of input signals of the gate, it is also called the fan-in of the gate. This door has a fan-in of 3.

4) The fan-out as shown schematically in the figure below represents the maximum that an S output of a logic gate can handle used as inputs for the next logic gates. The fan-out in the figure is 3, so the gate cannot provide its output S as an input for more than 3 other logic gates. However, its can handle less than 3.

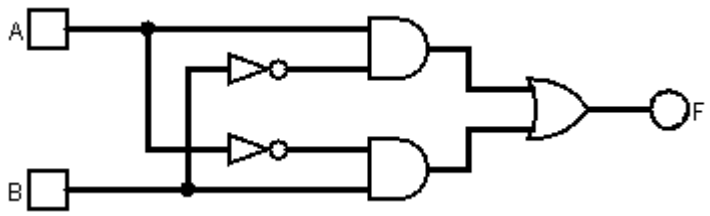


Exercise 02 :

A.	Valid.
B.	Invalid, it doesn't respect rule number 5, it contains a cycle (a loop).
C.	Valid.
D.	Invalid, it doesn't respect rule number 4, a signal can only have one starting point. Otherwise the 2 outputs may have 0 (0 volts) for one end and (5 volts) for the other on the same wire, electrically this represents a short circuit, which can damage the circuit.
E.	Invalid, it doesn't respect rule number 5, it contains a cycle (a loop).
F.	Valid.

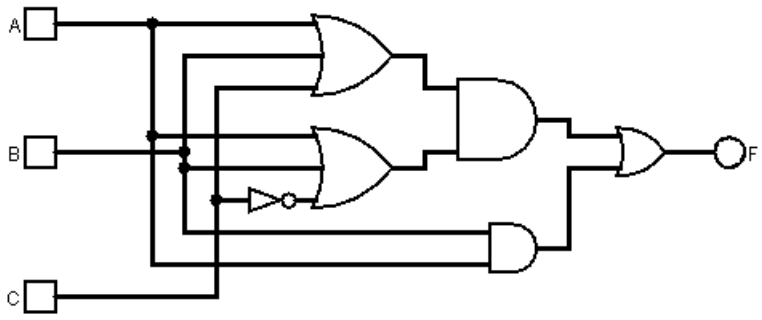
Exercise 03 :

1) $F(A,B) = A\cdot\overline{B} + \overline{A}\cdot B$



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

2) $F(A,B,C) = (A+B+C)\cdot(A+B+\overline{C})+A\cdot B$

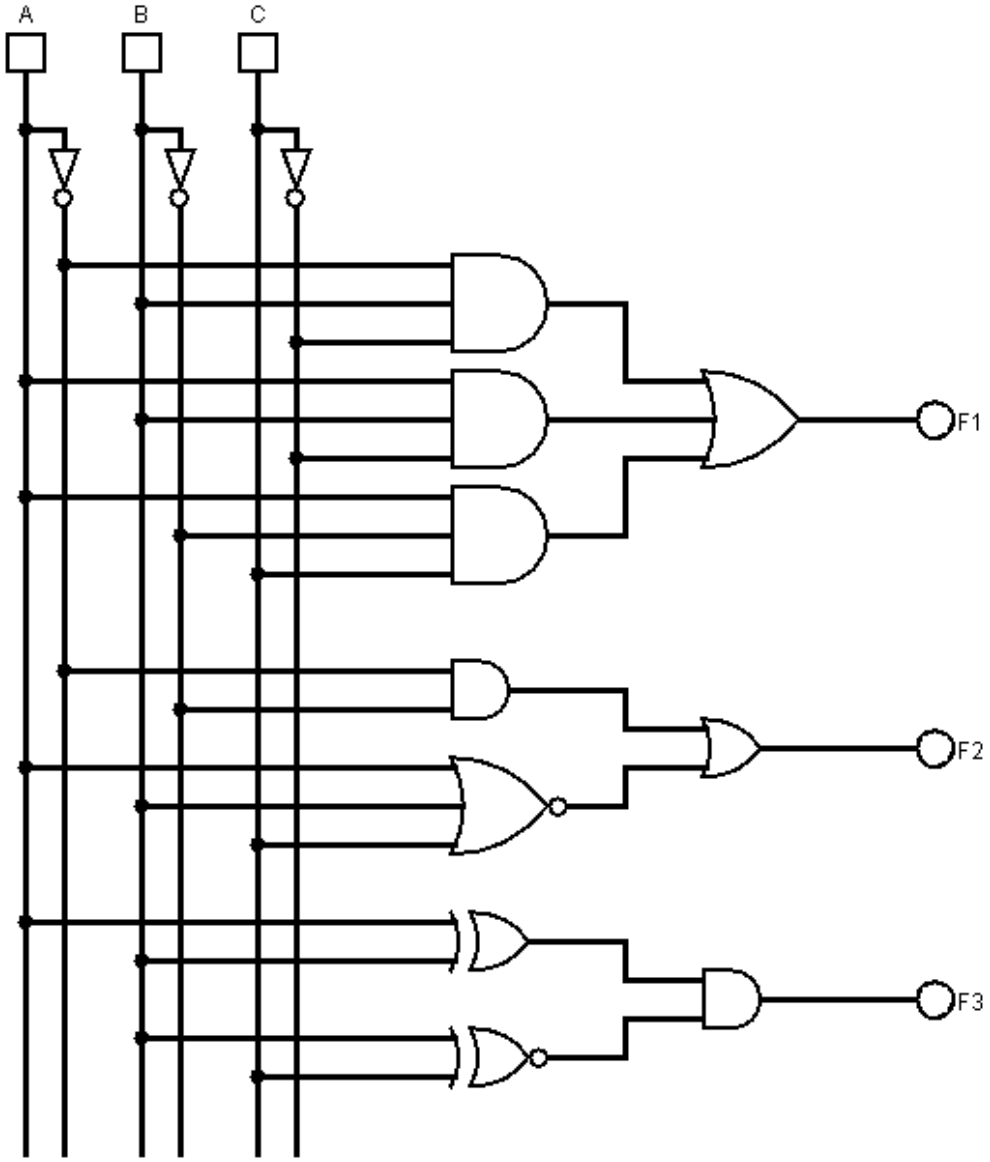


A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3) $F_1(A,B,C) = \overline{A}\cdot B\cdot\overline{C} + A\cdot B\cdot\overline{C} + A\cdot\overline{B}\cdot C$

$F_2(A,B,C) = \overline{A}\cdot\overline{B} + \overline{A+B+C}$

$F_3(A,B,C) = (A \oplus B)\cdot(B \otimes C)$



A	B	C	F1	F2	F3
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	0	0	0