Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2024/25)
Machine Structures 2 course
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Machine Structures 2 exam solution

Exercise 1 : (4 points)

1. The purpose of studying Digital Electronics in a Computer Science course is to understand the fundamental hardware principles and building blocks upon which computers and their components are designed and operate. **(1 point)**

2. A Multiplexer selects/chooses one of several input signals and forwards the selected input to a single output line. **(1 point)**

3. The input 1011 has three '1's, which is an odd number. Therefore, the Parity Controller would output 1. **(1 point)**

4. After the first rising edge on a JK-FlipFlop with (J, K) = (1,0) :
Q = 1
$\overline{Q}$ = 0 **(0.5 point)**
After the second rising edge with (J, K) = (1,1) :
Q = 0
$\overline{Q}$ = 1 **(0.5 point)**

Exercise 2 : (5 points + 1 bonus)

1. 5-steps method :
Step 2 : Truth Table **(1.5 point)**

E3	E2	E1	E0	P1	P0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1

1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

Step 3 : Conjunctive Canonical Functions **(0.75 point)**

P1(E3,E2,E1,E0) = $(E3+E2+E1+E0)\cdot(E3+E2+E1+\overline{E0})\cdot(E3+E2+\overline{E1}+E0)\cdot(E3+E2+\overline{E1}+\overline{E0})$

P0(E3,E2,E1,E0) = $(E3+E2+E1+E0)\cdot(E3+E2+E1+\overline{E0})\cdot(E3+\overline{E2}+E1+E0)\cdot(E3+\overline{E2}+E1+\overline{E0})\cdot$
$(E3+\overline{E2}+\overline{E1}+E0)\cdot(E3+\overline{E2}+\overline{E1}+\overline{E0})$

V(E3,E2,E1,E0) = $(E3+E2+E1+E0)$

Step 4 : Karnaugh Map **(0.75 point)**

E1E0 \ E3E2	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

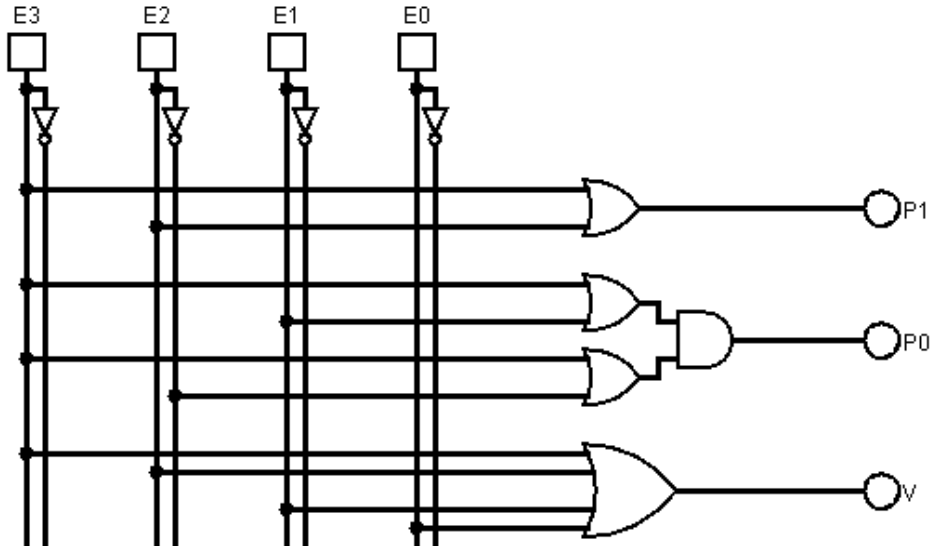
E1E0 \ E3E2	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	1	0	1	1
10	1	0	1	1

P1(E3,E2,E1,E0) = E3+E2

P0(E3,E2,E1,E0) = $(E3+E1)\cdot(E3+\overline{E2})$

V(E2,E1,E0) = E3+E2+E1+E0 (no more simplification possible)

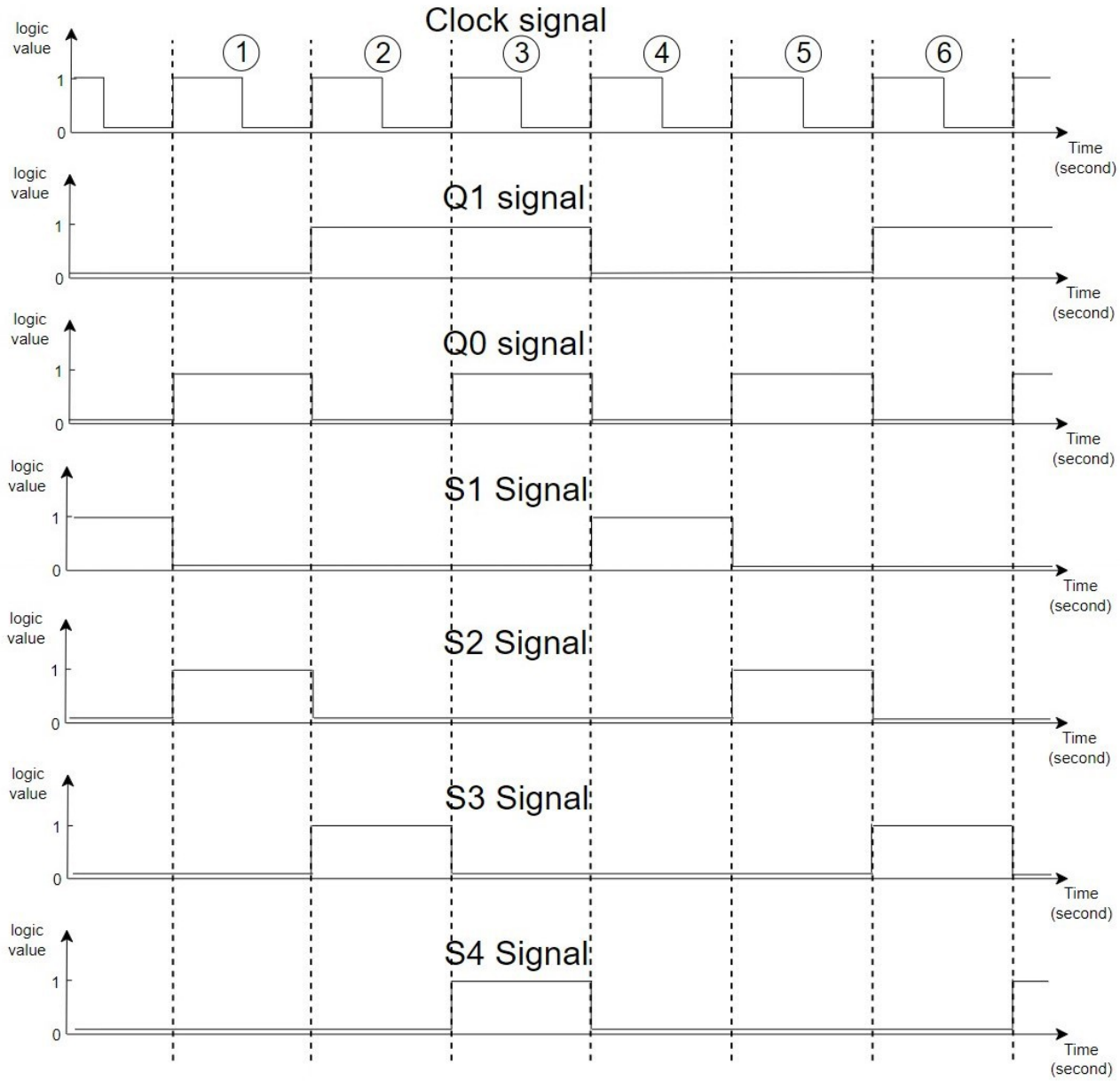
Step 5 : Schematics **(1 point)**



2. The input 0000 produces the output (P1, P0) = (0,0) and V = 0. **(0.5 point)**
and the input 0001 produces the output (P1,P0) = (0,0) and V = 1. **(0.5 point)**
That explains the V output purpose. It allows the differentiation between the absence of priority and the priority with level 0. **(1 point)**

Exercise 3 : (4 points)

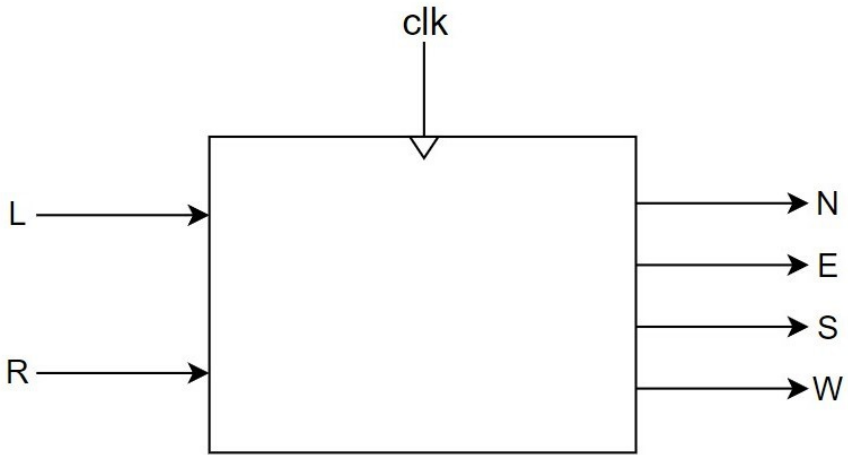
1. The timing diagram of the circuit : **(0.5 point for each cycle)**



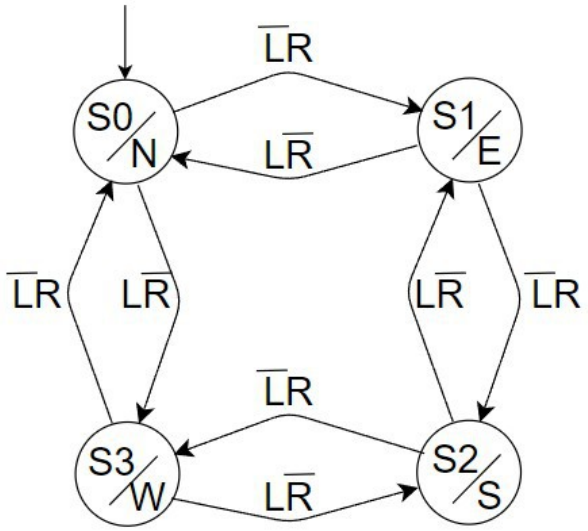
2. The 2 FlipFlops implement a 2 bits Counter. **(1 point)**

Exercise 4 : (7 points)

Step 1 : Global Scheme **(1 point)**



Step 2 : F.S.M. **(1 point)**



Note : The cases where L and R are not pressed, or they are pressed together at the same time, are not presented in the diagram for simplicity.

Step 3 : Transition Table **(1 point)**

Current State	L	R	Next State
S0	0	0	S0
S0	0	1	S1
S0	1	0	S3
S0	1	1	S0

S1	0	0	S1
S1	0	1	S2
S1	1	0	S0
S1	1	1	S1
S2	0	0	S2
S2	0	1	S3
S2	1	0	S1
S2	1	1	S2
S3	0	0	S3
S3	0	1	S0
S3	1	0	S2
S3	1	1	S3

Step 4 : Encoded States Table and Outputs Table **(1 point)**

State	S_1	S_0	N	E	S	W
S0	0	0	1	0	0	0
S1	0	1	0	1	0	0
S2	1	0	0	0	1	0
S3	1	1	0	0	0	1

Step 5 : Encoded Transition Table **(1 point)**

S_1	S_0	L	R	S'_1	S'_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	1	0

1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	1	0
1	1	1	1	1	1

Step 6 : Logical Functions **(1 point)**

$N(S_1,S_0) = \overline{S}_1 \cdot \overline{S}_0$
$E(S_1,S_0) = \overline{S}_1 \cdot S_0$
$S(S_1,S_0) = S_1 \cdot \overline{S}_0$
$W(S_1,S_0) = S_1 \cdot S_0$

LR \ S_1S_0	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	0	0	1	1
10	1	0	1	0

LR \ S_1S_0	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

$S'_1(S_1,S_0,L,R) = \overline{S}_1 \cdot S_0 \cdot \overline{L} \cdot R + \overline{S}_1 \cdot \overline{S}_0 \cdot L \cdot \overline{R} + S_1 \cdot \overline{L} \cdot \overline{R} + S_1 \cdot \overline{S}_0 \cdot R + S_1 \cdot S_0 \cdot L$
$S'_0(S_1,S_0,L,R) = S_0 \cdot \overline{L} \cdot \overline{R} + S_0 \cdot L \cdot R + \overline{S}_0 \cdot L \cdot \overline{R} + \overline{S}_0 \cdot \overline{L} \cdot R$

Step 7 : Schematics **(1 point)**