Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2024/25)
Machine Structures 2 course
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Machine Structures 2 resit exam solution

Exercise 1 : **(4 points)**

1. In Digital Electronics, information is fundamentally represented using the binary system, (relies only two distinct values 1 and 0, also considered correct). **(1 point)**

2. The Boolean expression for an XOR gate with inputs A and B and output S is :
$S = A \oplus B$ **(0.5 point)**

Truth Table of an XOR gate : **(0.5 point)**

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

3. A D-Latch is transparent when the clock is at 1. **(0.5 point)**
And The D-FlipFlop is transparent while the rising edge (or passing from 0 to 1) of the clock. **(0.5 point)**

4. The values inside the FlipFlops register of a Sequential Circuit represent the encoding States of the F.S.M related to the Sequential Circuit. **(1 point)**

Exercise 2 : **(5 points)**

5-step method to design the Decoder 4-2 :

Step 2 : Truth Table **(1 point)**

E1	E0	S0	S1	S2	S3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

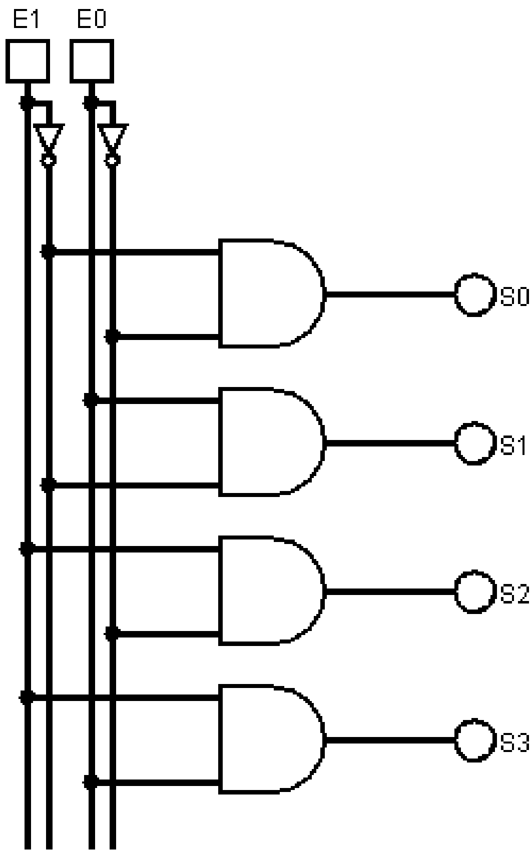
Step 3 : Canonical Disjunctive Functions **(1 point)**

S0(E1,E0) = $\overline{E1}\cdot\overline{E0}$
S1(E1,E0) = $\overline{E1}\cdot E0$
S2(E1,E0) = $E1\cdot\overline{E0}$
S3(E1,E0) = $E1\cdot E0$

Step 4 : Karnaugh Map

No more simplification is possible.

Step 5 : Schematics **(1 point)**



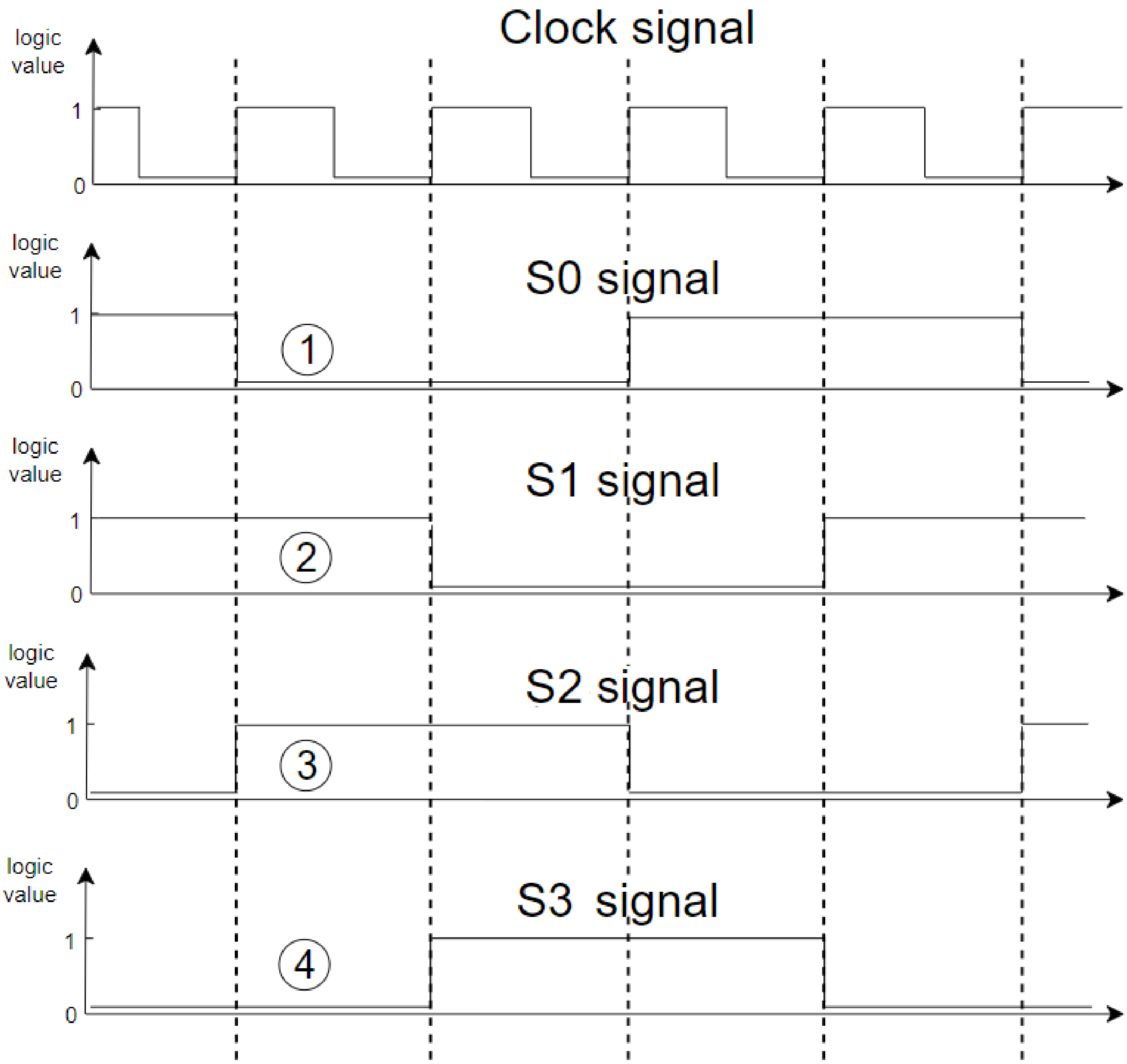
1. Inputs : (E1,E0) = (0,0) and (In3,In2,In1,In0) = (0,0,0,1), the circuit *output* = 1 **(0.5 point)**

Inputs : (E1,E0) = (1,1) and (In3,In2,In1,In0) = (1,1,1,1), the circuit *output* = 1 **(0.5 point)**

2. The circuit created in the schematics is a : Mutiplexer 4-1 **(1 point)**

Exercise 3 : **(4 points + 1 point)**

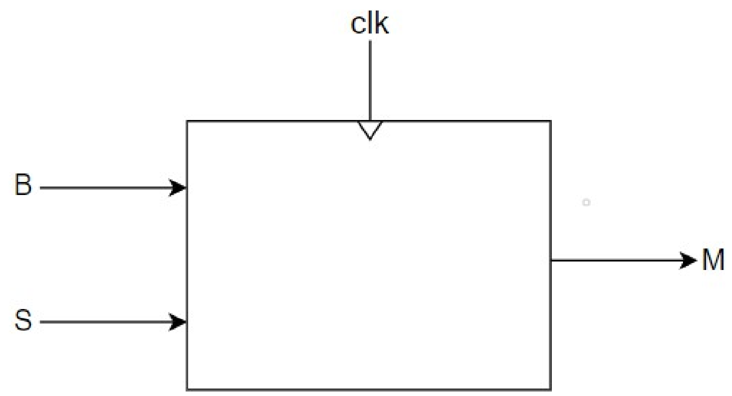
1. The timing diagram of the circuit : **(1 point for each signal)**



2. Name the circuit is : <u>Circular SIPO Shifter</u>. (same meaning as <u>Circular</u> is accepted) **(1 point)**

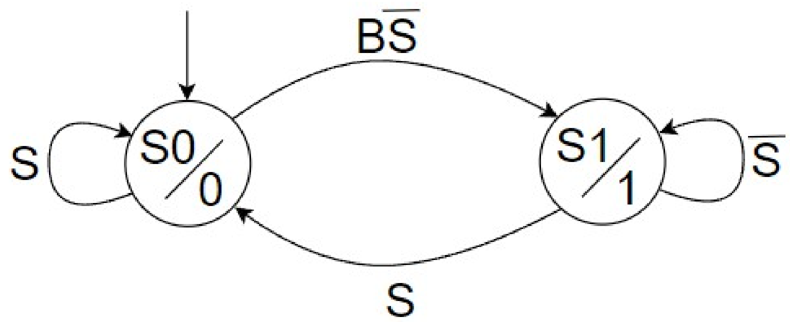
Exercise 4 : **(7 points)**

Step 1 : Global Scheme **(1 point)**



B : Button
S : Sensor
M : Motor

Step 2 : F.S.M. **(1 point)**



Note : Only the most important transitions are depicted in the F.S.M.

Step 3 : Transition Table **(1 point)**

Current State	B	S	Next State
S0	0	0	S0
S0	0	1	S0
S0	1	0	S1
S0	1	1	S0
S1	0	0	S1
S1	0	1	S0
S1	1	0	S1
S1	1	1	S0

Step 4 : Encoded States Table and Outputs Table **(1 point)**

State	S_t	M
S0	0	0
S1	1	1

Note : We name the state encoding S_t to make it different from S, the sensor input.

Step 5 : Encoded Transition Table **(1 point)**

S_t	B	S	S_t'
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Step 6 : Logical Functions **(1 point)**

$M(S_t)$ = S_t (directly extracted)

S_t \ B S	00	01	11	10
0	0	0	0	1
1	1	0	0	1

$S_t'(S_t,B,S) = B\cdot\overline{S} + S_t\cdot\overline{S}$

Step 7 : Schematics **(1 point)**